REMARKS

The Office Action dated September 7, 2005, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Restriction Requirement

In view of the telephonic restriction requirement dated August 18, 2005, the Applicants withdraw claims 1-4 and 6 from further examination, and confirm the election of Invention II directed to claim 5, 7-8 of the present application.

Rejection of Claims 5, 7-8 Under 35 U.S.C. § 102(b)

The Office Action rejected claims 5, 7-8 under 35 U.S.C. § 102(b) as being anticipated by Parmenter et al. (U.S. Patent No. 5,679,353, hereinafter "Parmenter"). The Applicants respectfully traverse the rejection and submit that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

It is submitted that Parmenter teaches a clock switching method, switching between a basic and PLL clock signal where the method includes waiting until the next clock phase boundary to switch the clocks.

In characterizing Parmenter, the Examiner takes the position that the "waiting" in Parmenter is the equivalent of the functional feature of "counting" as recited in claim 5.

The Applicants respectfully disagree and submit that Parmenter fails to teach any relation between the counting period and the frequency difference of the basic clock and PLL clock, as claimed in claim 5.

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For example, claim 5 of the present invention recites the limitations of "inhibiting outputting the basic clock signal upon receiving the switch signal; counting a predetermined number of the PLL clock signal after inhibiting outputting the basic clock signal; ... wherein the predetermined number is set according to the frequency difference between the basic clock frequency and the PLL clock frequency."

In addition, claim 8 recites "an inhibiting circuit that inhibits said fast clock within a term depends on a difference between said frequency of said basic clock and said frequency of said fast clock in the case of switching said output from said basic clock to said fast clock."

In contrast, Parmenter fails to teach or suggest the functional relationship between inhibiting the outputting of the basic clock signal and the frequency difference between the two clocks as disclosed in one exemplary embodiment of the present invention. In other words, Parmenter fails to disclose at least the limitation of "wherein the predetermined number is set according to the frequency difference between the basic clock frequency and the PLL clock frequency," as recited in claim 5 and "an inhibiting circuit that inhibits said fast clock within a term depends on a difference between said frequency of said basic clock and said frequency of said fast clock in the case of switching said output from said basic clock to said fast clock," as recited in claim 8.

Furthermore, the Applicants submit that the "waiting" until the next clock phase boundary to change in Parmenter is neither comparable nor analogous to the functional features of "counting a predetermined number of the PLL clock signal after inhibiting

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outputting the basic clock signal; ... wherein the predetermined number is set according to the frequency difference between the basic clock frequency and the PLL clock frequency," as recited in the present invention. Therefore, Applicants submit that Parmenter fails to disclose each and every element recited in claims 5 and 8 of the present application.

As for claims 7 and 8, the Office Action characterizes Parmenter as allegedly disclosing,

> a PLL circuit (figure 2, structure 15) that generates a fast clock (figure 2, node 2X_CLK2) whose frequency is more than twice as much as a frequency of the basic signal (figure 2, node 17). ... [f]Further discloses multiplexers and their associated control means (figure 2, structures 19, 21, and their control means structure SR1), which are equivalent to the claimed inhibiting circuit that inhibits said fast clock by a time (figure 2, the logic circuit node 27, column 2, lines 11-19)...

In particular, the Office Action characterizes the "multiplexers and their associated control means (figure 2, structures 19, 21, and their control means structure SR1)" of Parmenter as allegedly being comparable to the feature of "inhibiting circuit that inhibits said fast clock ..." recited in claims 7 and 8 of the present application.

The Applicants respectfully disagree and traverse the Examiner's position.

For instance, the Applicants submit that Parmenter fails to disclose or suggest each and every element recited in claims 7 and 8 of the present application. In particular, it is submitted that the "multiplexers and their associated control means" of Parmenter are neither comparable nor analogous to the "inhibiting circuit that selects said fast clock in response to a connecting of an interface cable and inhibits said first

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clock in response to a disconnecting of the interface cable," nor comparable nor analogous to the "inhibiting circuit that inhibits said fast clock ...," of claims 7 and 8 of the present application, respectively.

In one example of the present invention, the fast clock and the basic clock are switched depending on the connecting or disconnecting of the interface cable. In contrast, Parmenter switches the reference clock and PLL clock depending on lock or unlock condition of PLL, and NOT depending on the connection or disconnection of the interface cable of the present invention. Therefore, the Applicants submit that Parmenter also fails to disclose each and every element recited in claims 7 and 8 of the present application.

In order to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Parmenter fails to disclose or suggest each and every feature of claims 5, 7 and 8. Accordingly, the Applicants respectfully submit that claims 5, 7 and 8 are not anticipated by nor rendered obvious by the disclosure of Parmenter. Therefore, the Applicants respectfully submit that claims 5, 7 and 8 are allowable.

Accordingly, the Applicants respectfully request withdrawal of the rejection.

Rejection of Claim 5 Under 35 U.S.C. § 103(a)

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Yokogawa et al. (U.S. Patent No. 4,872,155, hereinafter "Yokogawa") in view of Ishikawa (U.S. Patent No. 6,346,830). The Applicants respectfully traverse the rejection.

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In making the rejection, the Office Action characterizes Yokogawa as allegedly teaching "counting the clock signal, inhibiting the clock output, and output PLL clock signal after a predetermined number of clock signal," and cites column 4, lines 59-64; column 5, lines 4-6, Figure 10 for support.

The Applicants respectfully disagree since Yokogawa merely teaches a counter that detects the pulse spacing of the clock data to supply the PLL circuit with a signal corresponding to the basic clock so that the PLL clock data is in synchronism with the basic clock. (See, Yokogawa Column 4 Line 59-Column 5 Line 6). Therefore, the Applicants submit that the "counter that detects the pulse spacing of the clock data" of Yokogawa is clearly distinguishable from the processes recited in claim 5 of "counting a predetermined number of the PLL clock signal after inhibiting outputting the basic clock signal . . . wherein the predetermined number is set according to the frequency difference between the basic clock frequency and the PLL clock frequency."

Hence, it is submitted that Yokogawa merely teaches counting the basic clock data rather than the PLL clock signal as recited in the present claim 5. Accordingly, Yokogawa fails to teach at least inhibiting the clock signal, but rather teaches synchronizing the basic clock data and the PLL clock data.

Ishikawa fails the cure the deficiencies discussed above with respect to Yokogawa. Accordingly, the Applicants respectfully submit that Yokogawa in view of Ishikawa fails to disclose or suggest each and every features recited in claim 5 of the present application and therefore is allowable.

Conclusion

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In view of the above, Applicants respectfully submit that each of claims 5, 7-8 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 5, 7-8 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time.

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Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, referring to client-matter number 108066-00018.

Respectfully submitted,
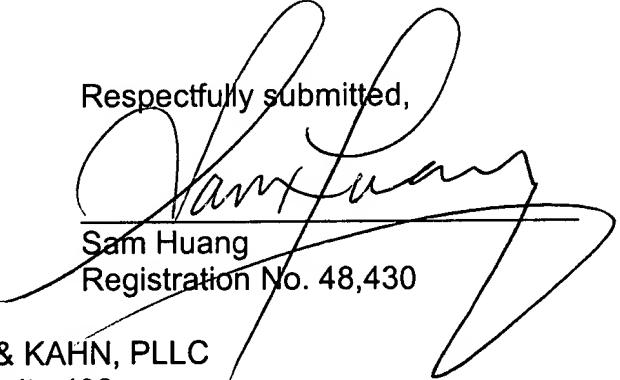
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Enclosure: Petition for Extension of Time (three months)

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